Andrew Sykes

Design Verification and RTL Design | La Mirada, CA | (714) 345-2318 | sykes.andrew21@gmail.com | linkedin.com/in/atsykes | atsykes.com

Education

M.S. Computer Engineering | University of Southern California — May 2027

B.S. Computer Engineering and Computer Science | University of Southern California — December 2026

- Major GPA: 3.6 | Viterbi Dean's List | Coursework: VLSI System Design, MOS VLSI Design, Computer Architecture

Technical Skills

Languages: Verilog, C/C++, Python
Design Verification: Self-checking testbenches, constrained-random stimulus, scoreboarding, directed testing
Digital Design: RTL design, FSMs, round-robin arbitration, virtual channels, flow control, Network-on-Chip (NoC)
EDA and Tools: Cadence Virtuoso, QuestaSim, Icarus Verilog, Xilinx Vivado, KiCad, Git
Hardware: Nexys Artix-7 FPGA, ATmega1284P, Teensy, Arduino, Raspberry Pi, SPI, I2C, PCB debug

Projects

Network-on-Chip Router for a 4x4 Mesh Multicore | *Verilog* — August 2026 – Present

- Designed a 5-port packet-based router in synthesizable Verilog, extending a 2-direction ring spec to a 4x4 mesh with two virtual channels, round-robin arbitration, 2-cycle hop latency, back-pressure flow control, and deadlock-free XY routing.
- Integrated 16 routers into a 4x4 mesh; an all-to-all test delivered 240 packets with zero loss, duplication, or corruption.
- Wrote 7 passing self-checking tests, including 400 constrained-random packets under random stalls checked by a scoreboard.

Pipelined 64-bit SIMD Processor and Microarchitecture Study | *Verilog, Design Compiler* — October 2026 – Present

- Co-designed a 4-stage 64-bit SIMD pipeline in Verilog; my EX/WB forwarding cut cycles 19%, passing 20,024 hazard checks.
- Moved the critical-path divider into a multi-cycle DesignWare unit: clock period from $\sim$100 ns to 1.9 ns, area down 24%.
- Designed a scoreboard for out-of-order completion past divides: best of 5 designs, up to 15.8$\times$ faster, +1.6% area.
- Co-ran a 5-design study on 20 benchmarks; I integrated an issue window that cut cycles 3% but slowed the clock up to 15%.

512-Bit 6T SRAM Array | *Cadence Virtuoso* — April 2026

- Built a 4x128-bit SRAM with abuttable custom bitcell layouts, sense amplifiers, row decoders, and precharge; DRC/LVS clean.

Semi-Custom Multiply-Accumulate (MAC) Datapath | *Cadence Virtuoso* — December 2025

- Designed a 16-bit MAC from custom D flip-flops, a carry-lookahead adder, radix-4 Booth encoders, and 3:2 and 6:2 compressors.

FPGA Game System | *Verilog, Nexys Artix-7, Xilinx Vivado, QuestaSim* — April 2025

- Developed a Verilog game with one-hot FSMs, VGA output, seven-segment displays, and physical I/O; synthesized in Vivado.

24hr Social, Embedded Automation System | *ATmega1284P, C, SPI, I2C* — May 2026

- Architected FSM-based firmware with a circular queue for RFID order tracking, sensing, and motor control across four stations.

Experience

DAQ Responsible Engineer | USC Liquid Propulsion Laboratory, Los Angeles, CA — April 2026 – Present

- Serve as sole DAQ operator during liquid engine hot-fire tests, owning real-time data collection and system readiness.
- Troubleshoot DAQ hardware using PCB schematics and electrical measurements to isolate wiring and component faults.
- Promoted from Data Acquisition and Controls member (February 2026); assembled strain-gauge circuits for tank burst tests.

Global Supply Chain Intern | Northrop Grumman, El Segundo, CA — June 2026 – August 2026

- Evaluated supplier cybersecurity compliance against NIST SP 800-171, FAR 52.204-21, and DFARS 252.204 for FCI and CUI.
- Resolved compliance gaps delaying purchase orders and helped build an internal cybersecurity guidance website for buyers.

Research Assistant | Autonomous Networks Research Group, USC — February 2025 – May 2025

- Built a Python pipeline to generate DAG workloads and benchmark task schedulers (HEFT, CPoP, SDBATS) by makespan.

Electrical Engineering Course Producer | USC Viterbi School of Engineering — August 2024 – May 2025

- Supported 150+ EE and CS students in embedded systems; assisted labs on combinational and sequential logic and FSMs.